Fig.1

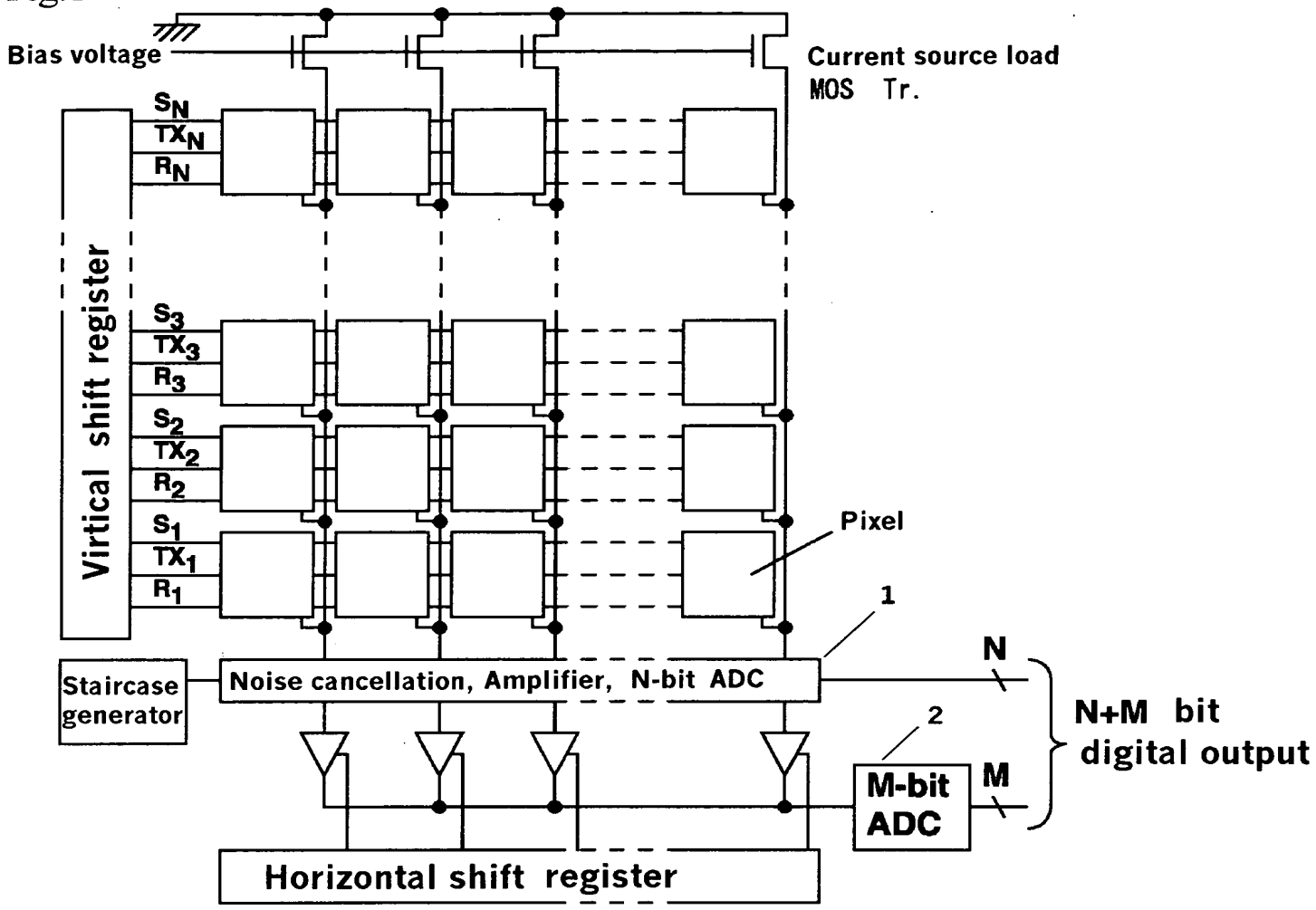

Bias voltage
Current source load MOS Tr.
S_N
TX_N
R_N
Virtical shift register
S_3
TX_3
R_3
S_2
TX_2
R_2
S_1
TX_1
R_1
Pixel
1
Staircase generator
Noise cancellation, Amplifier, N-bit ADC
N
2
M-bit ADC
M
N+M bit digital output
Horizontal shift register

Fig.2

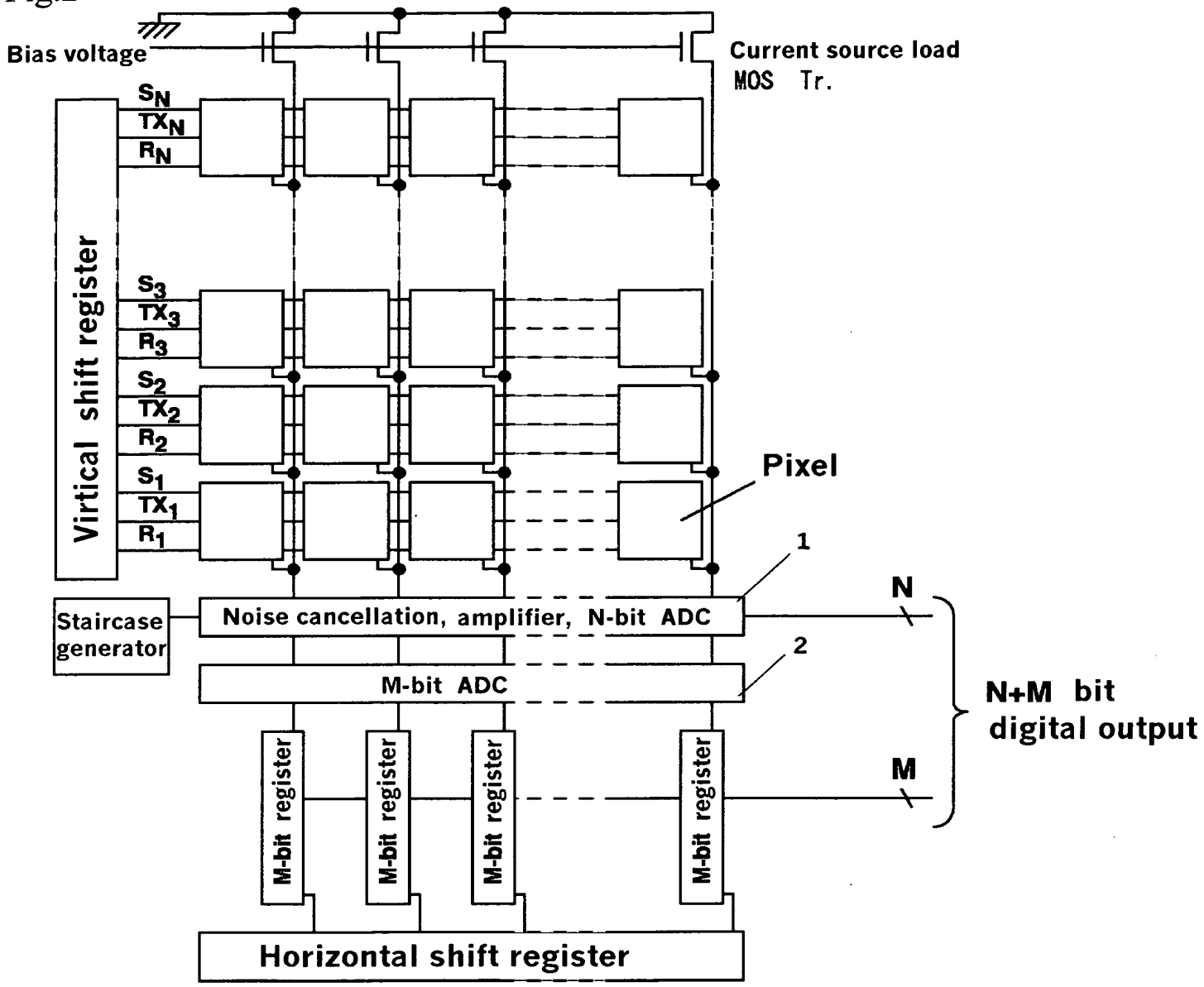

Bias voltage
Current source load MOS Tr.
Virtical shift register
S_N
TX_N
R_N
S_3
TX_3
R_3
S_2
TX_2
R_2
S_1
TX_1
R_1
Pixel
1
N
Staircase generator
Noise cancellation, amplifier, N-bit ADC
2
M-bit ADC
N+M bit digital output
M
M-bit register
M-bit register
M-bit register
M-bit register
Horizontal shift register

Fig.3

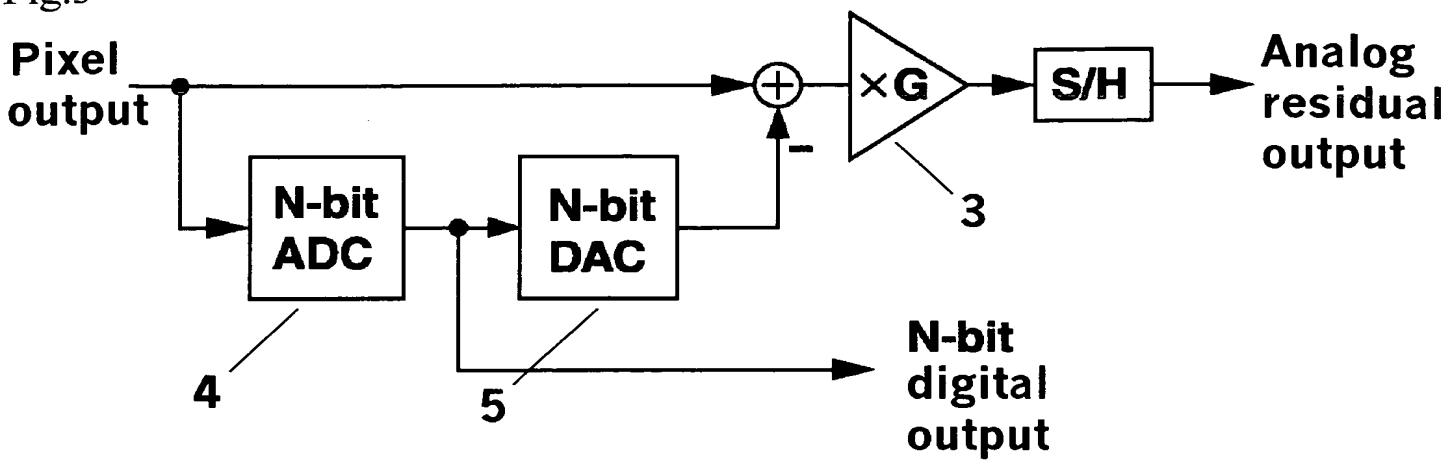

Pixel output
×G
S/H
Analog residual output
N-bit ADC
N-bit DAC
3
4
5
N-bit digital output

Fig.4

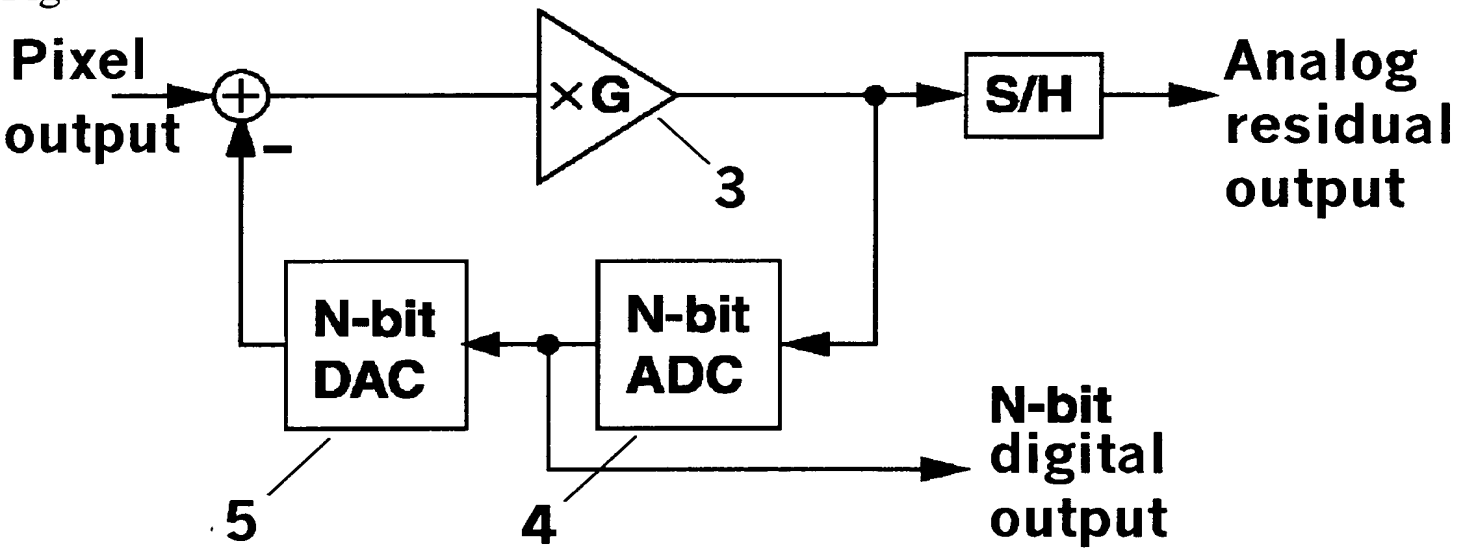

Pixel output
×G
S/H
Analog residual output
3
N-bit DAC
N-bit ADC
5
4
N-bit digital output

Fig.5

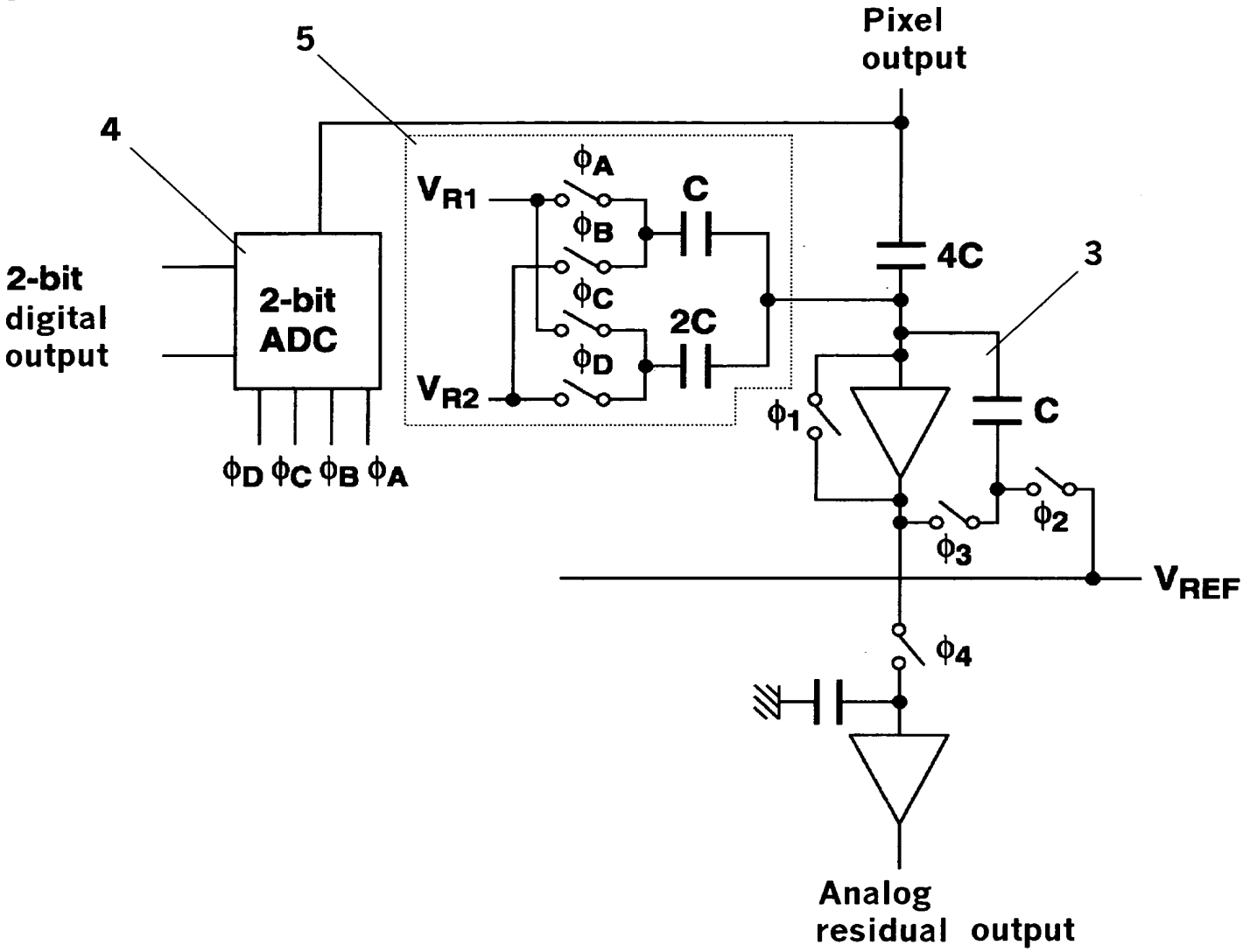

Pixel output
5
4
ϕ_A
V_{R1}
ϕ_B
C
ϕ_C
2C
ϕ_D
V_{R2}
4C
3
2-bit digital output
2-bit ADC
ϕ_1
C
ϕ_2
ϕ_3
V_{REF}
ϕ_4
ϕ_D ϕ_C ϕ_B ϕ_A
Analog residual output

Fig.6

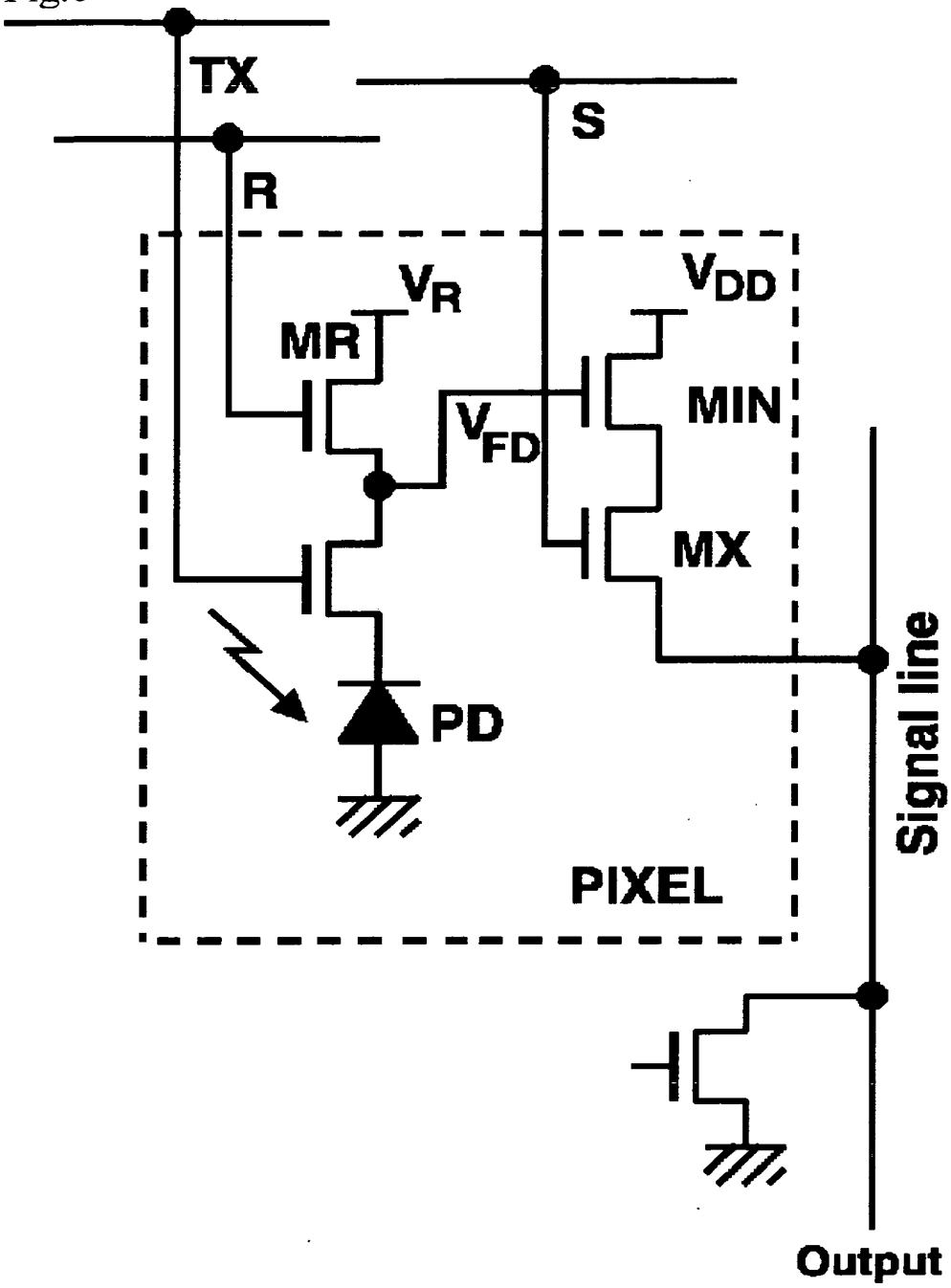


Fig.7

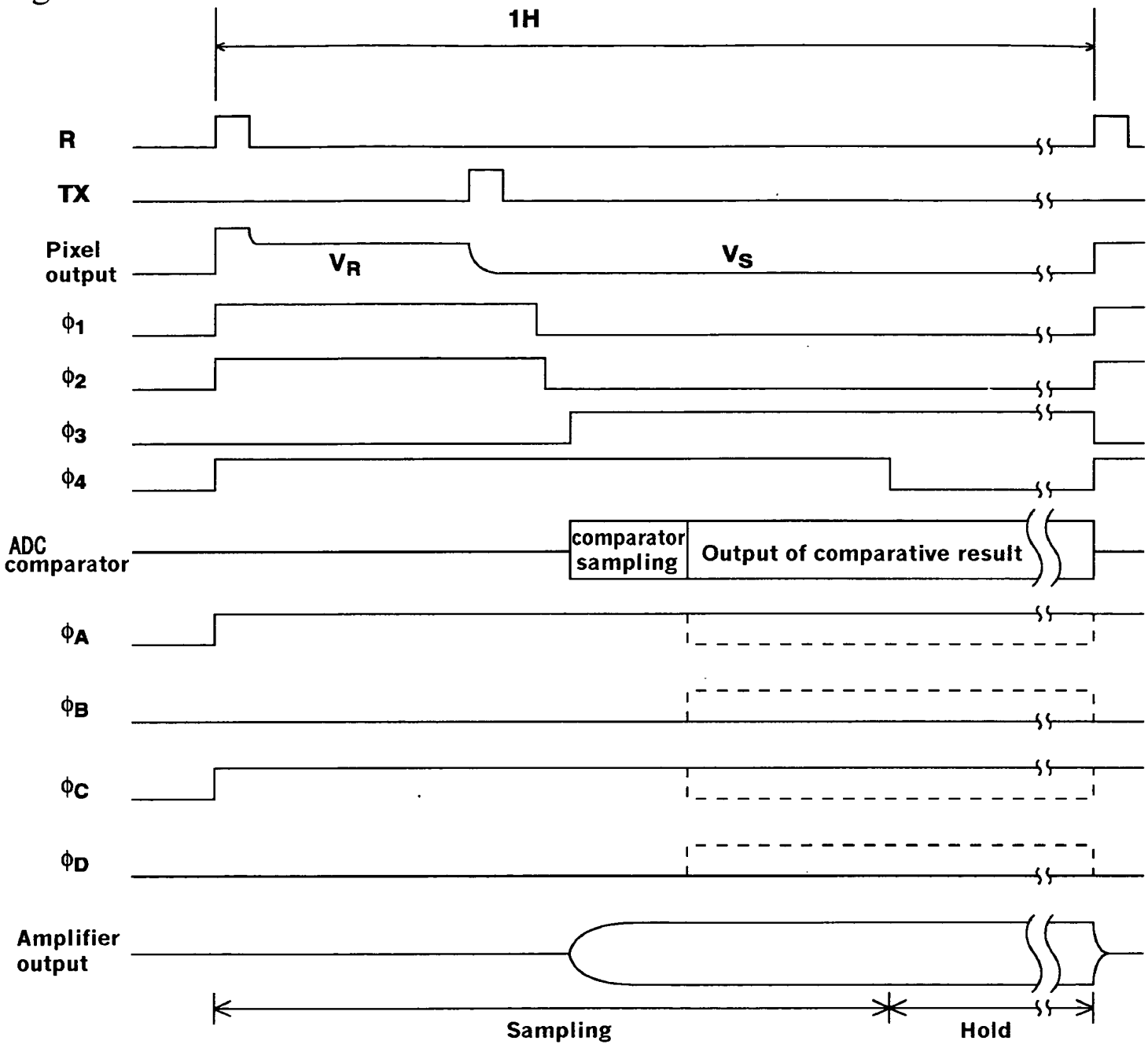

1H
R
TX
Pixel output
V_R
V_S
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ADC comparator
comparator sampling
Output of comparative result
ϕ_A
ϕ_B
ϕ_C
ϕ_D
Amplifier output
Sampling
Hold

Fig.8

D	ϕA	ϕB	ϕC	ϕD
0	1→1	0→0	1→1	0→0
1	1→0	0→1	1→1	0→0
2	1→1	0→0	1→0	0→1
3	1→0	0→1	1→0	0→1

Fig.9

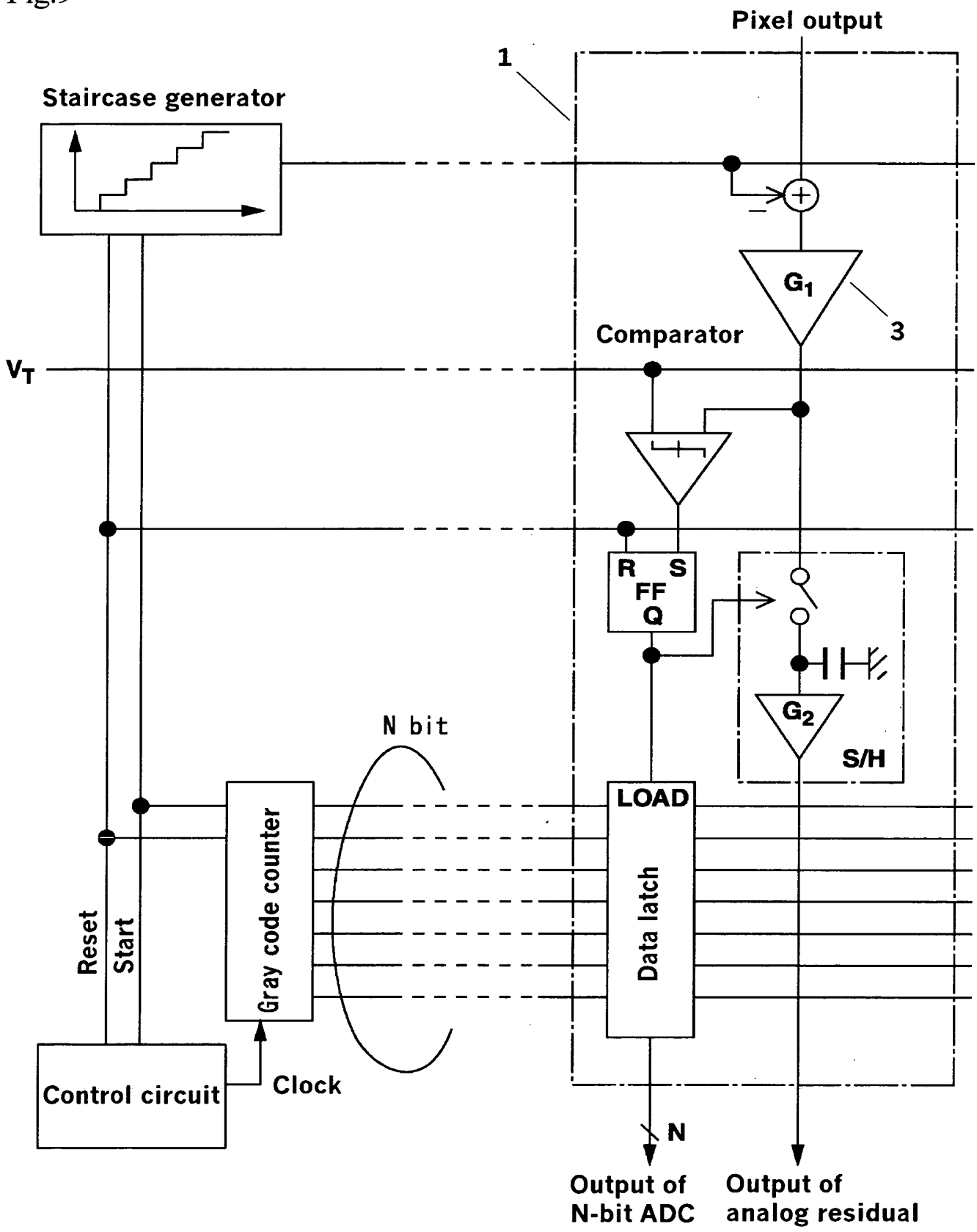

Pixel output
1
Staircase generator
G_1
3
Comparator
V_T
R S
FF
Q
G_2
S/H
N bit
LOAD
Data latch
Gray code counter
Reset
Start
Control circuit
Clock
N
Output of
N-bit ADC
Output of
analog residual

Fig.10

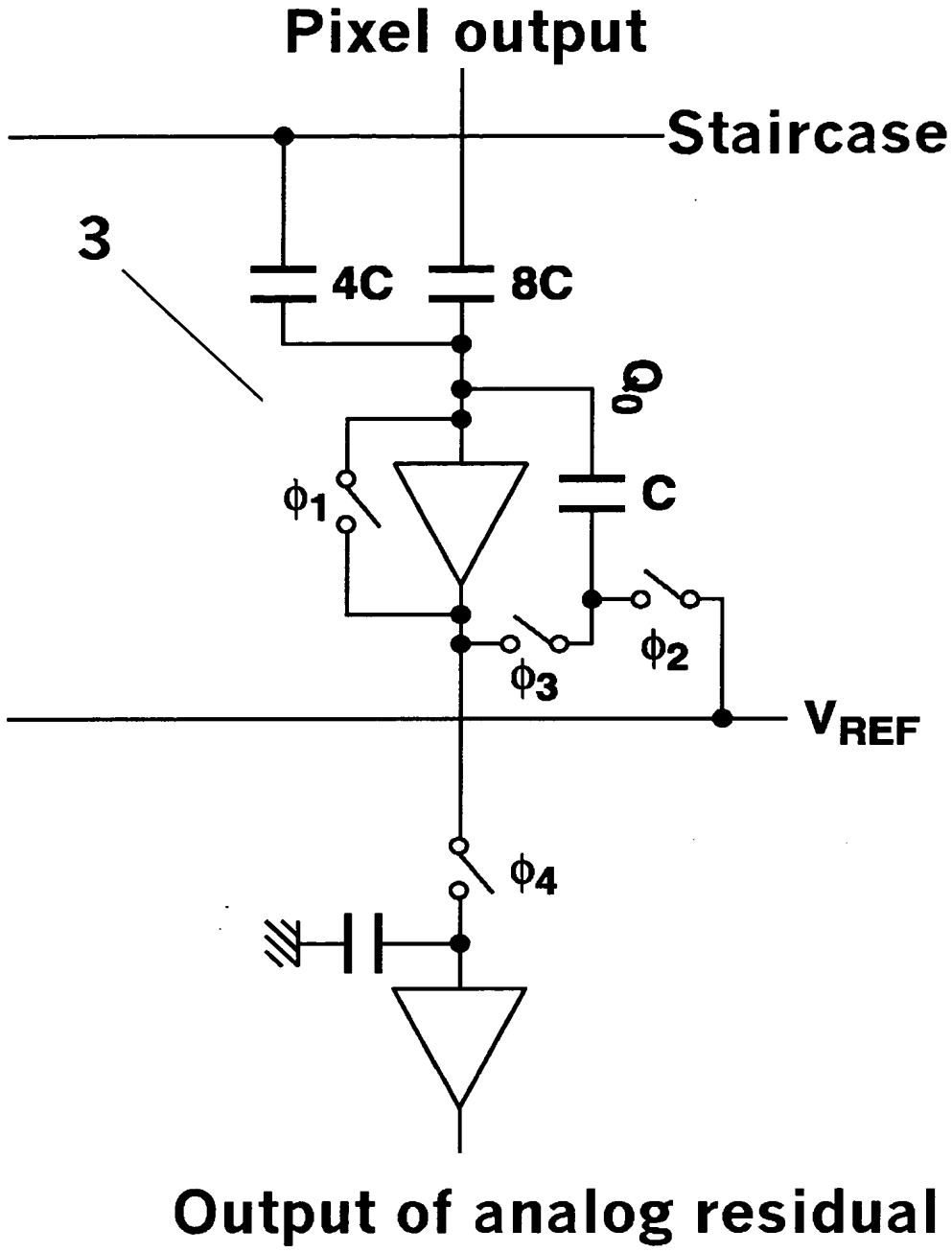

Pixel output
Staircase
3
4C
8C
C_0
C
ϕ_1
ϕ_2
ϕ_3
ϕ_4
V_{REF}
Output of analog residual

Fig.11

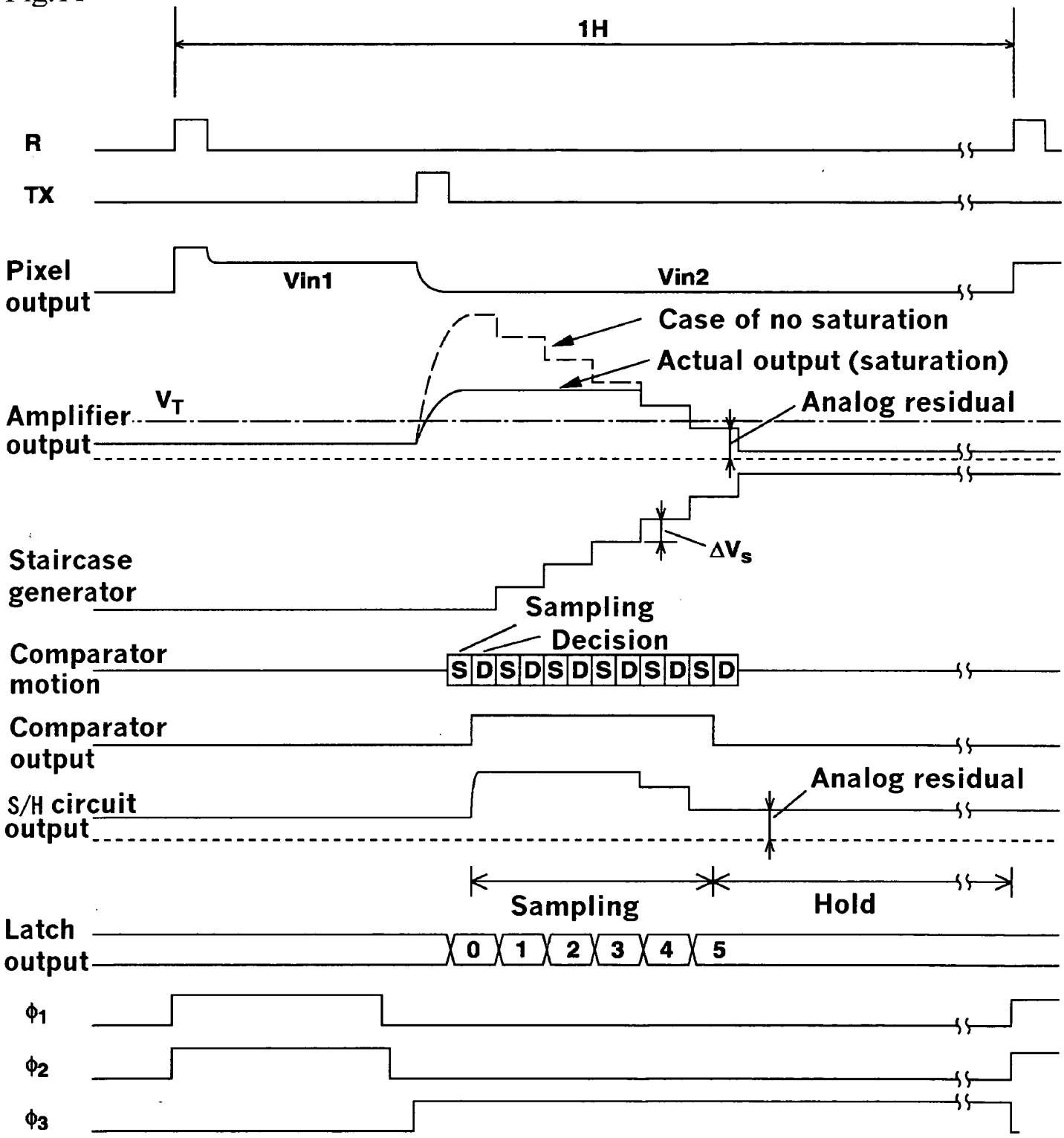

1H
R
TX
Pixel output
Vin1
Vin2
Case of no saturation
Actual output (saturation)
Amplifier output
V_T
Analog residual
ΔV_S
Staircase generator
Sampling
Decision
Comparator motion
S D S D S D S D S D S D
Comparator output
Analog residual
S/H circuit output
Sampling
Hold
Latch output
0 1 2 3 4 5
ϕ_1
ϕ_2
ϕ_3

Fig.12

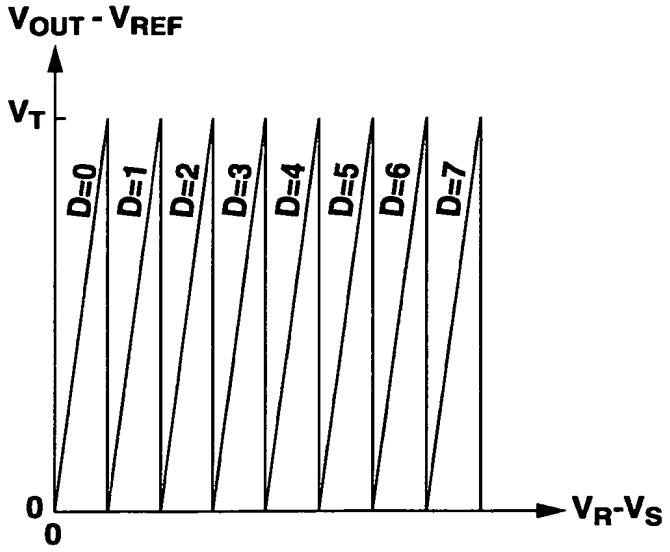

VOUT - VREF
VT
D=0
D=1
D=2
D=3
D=4
D=5
D=6
D=7
0
0
VR-VS

Fig.13

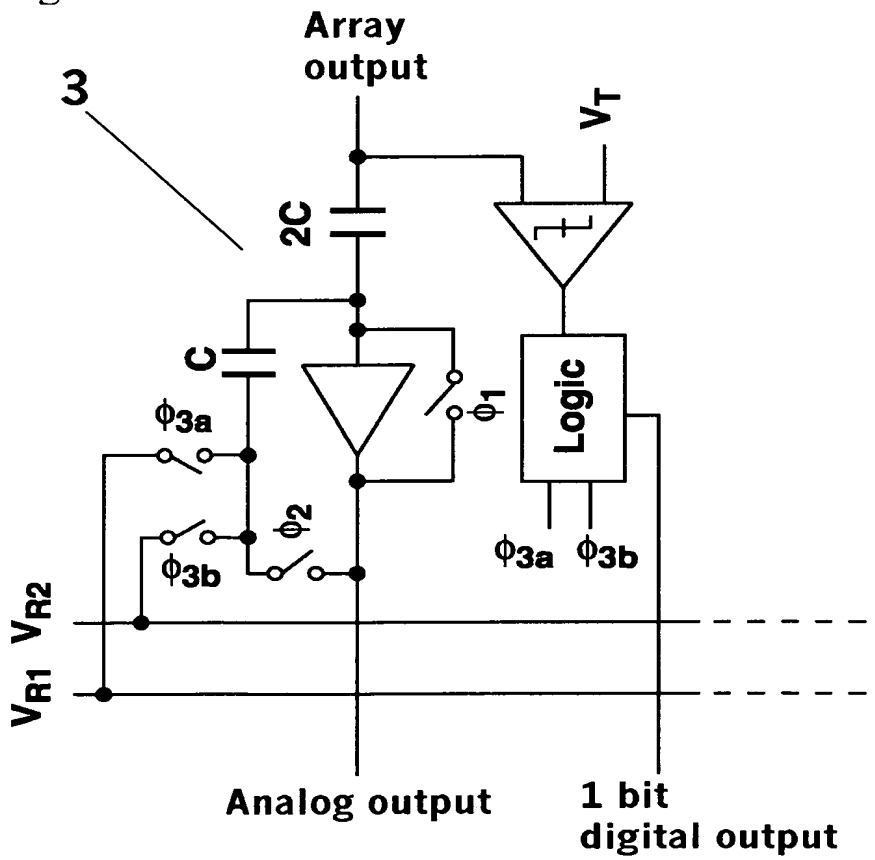

Array output
3
VT
2C
C
Logic
φ1
φ3a
φ2
φ3b
φ3a φ3b
VR2
VR1
Analog output
1 bit digital output

Fig.14

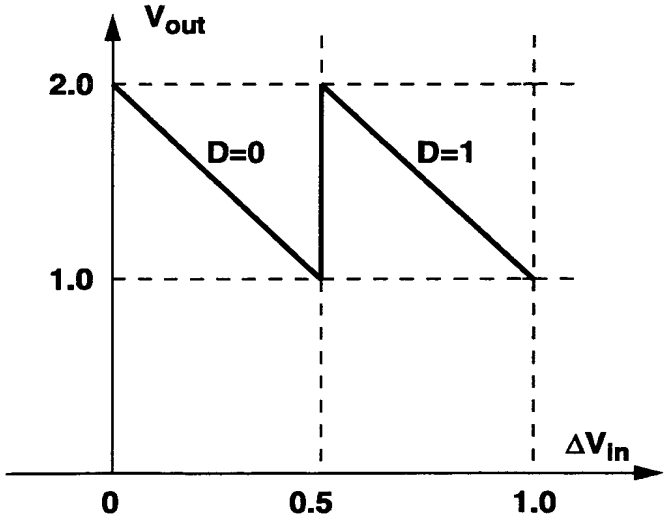
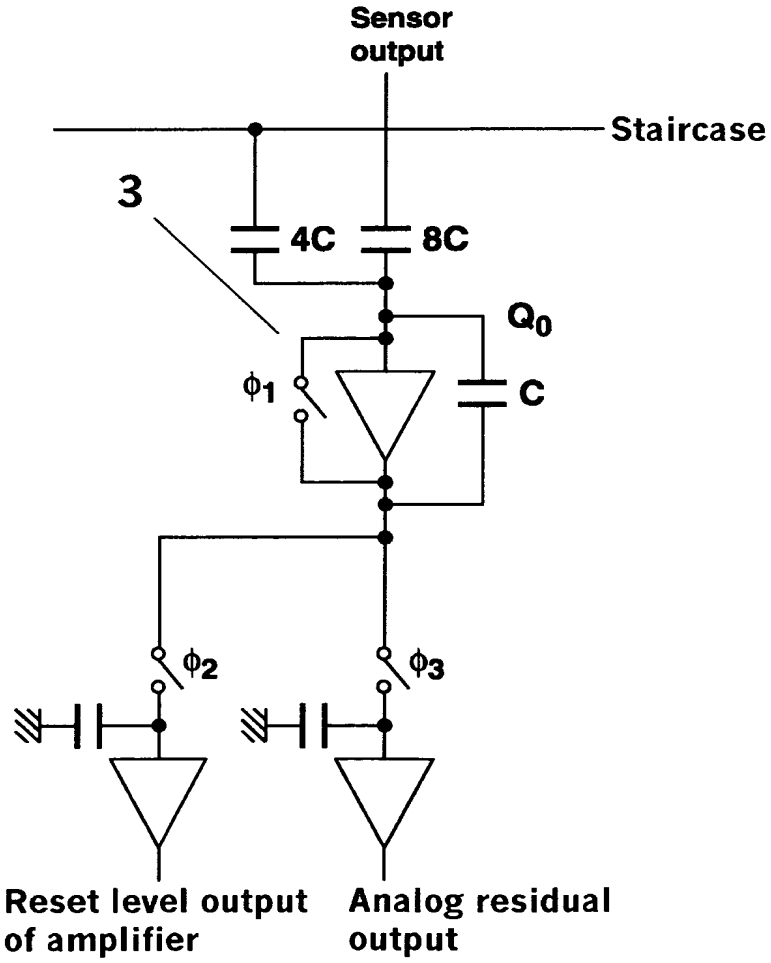

Vout
2.0
1.0
D=0
D=1
ΔVin
0
0.5
1.0

Fig.15


Sensor output
Staircase
3
4C
8C
Q0
ϕ1
C
ϕ2
ϕ3
Reset level output of amplifier
Analog residual output